Abstract of the Disclosure

An multi-threading processor is provided. The multi-threading processor includes a front end module, an execution module coupled to the front end module, and a state module coupled to both the front end module and the execution module. The processor also includes a switch logic module, which is coupled to the state module. The switch logic module detects switching events and mispredicted branches and conceals switch latency by attempting to schedule switches to other software threads during the latencies of the mispredicted branches.